AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please cancel claim 8 without prejudice and amend claims 3, 5, 7 and 11 as follows:

LISTING OF CLAIMS:

1. (Canceled)

2. (Canceled)

3. (Currently Amended) A data processor with a hardware repeat function which executes ~~a program including~~ a repeat block composed of plural instructions N times (N is an integer equal to or more than 0) repeatedly, and stops the repeat processing after processing a designated instruction in a N+1 th repeat processing, independently of an operation specified by an instruction being executed ~~and processed repeatedly~~, said data processor comprising:

a detecting ~~means implemented by hardware,~~ unit for detecting that a processing instruction is said designated instruction and the repeat processing breaks after said designated instruction has been completed;

a first instruction processing sequence switching unit to switch the instruction processing sequence to a first instruction within the repeat block after a last instruction in the repeat block has been completed when the repeat processing is made to continue by a detection result of said detecting unit; and

a second instruction processing sequence switching unit to inhibit fetching of remaining instructions within the repeat block after completion of said designated instruction and to make fetching of a next instruction outside of said repeat block when the repeat processing is made to break by the detection result of said detecting unit ~~a break of repeat processing in said repeat block independently of an operation specified by an instruction being executed; and~~

~~instruction execution inhibit means responsive to the detection of said break of said repeat processing by said detecting means to inhibit execution of remaining instructions in said repeat block, wherein said instruction execution inhibit means is instruction processing sequence switching means for switching said instruction processing sequence to a next instruction of said repeat block at an instruction fetch stage upon detection of said break of said repeat processing by said detecting means~~.

4. (Canceled)

5. (Currently Amended) A data processor with a hardware repeat function which executes ~~a program including~~ a repeat block composed of plural instructions ~~and processed repeatedly~~ N times (N is an integer equal to or more than 0) repeatedly, and stops the repeat processing after processing a designated instruction in a N+1 th repeat processing, independently of an operation specified by an instruction being executed, said data processor comprising:

a detecting ~~means implemented by hardware,~~ unit for detecting that a processing instruction is said designated instruction and the repeat processing breaks after said designated instruction has been completed;

a first instruction processing sequence switching unit to switch the instruction processing sequence to a first instruction within the repeat block after a last instruction in the repeat block has been completed when the repeat processing is made to continue by a detection result of said detecting unit; and

a second instruction processing sequence switching unit to perform a jumping process to a next instruction outside of said repeat block by hardware, in parallel to executing said designated instruction and independently of an operation specified by said designated instruction when the repeat processing is made to break by the detection result of said detecting unit ~~a break of repeat processing in said repeat block independently of an operation specified by an instruction being executed; and~~

~~instruction execution inhibit means responsive to the detection of said break of said repeat processing by said detecting means to inhibit execution of remaining instructions in said repeat block, wherein said instruction execution inhibit means is instruction processing sequence switching means for switching said instruction processing sequence to a next instruction of said repeat block at an instruction execution stage upon detection of said break of said repeat processing by said detecting means, and~~

~~wherein said instruction processing sequence switching means is means for performing jump processing to the next instruction of said repeat block during execution of a last instruction that is executed last in said repeat processing of said repeat block~~.

6. (Canceled)

7. (Currently Amended) A data processor with a hardware repeat function which executes ~~a program including~~ a repeat block composed of plural instructions ~~and processed repeatedly~~ N times (N is an integer equal to or more than 0) repeatedly, and stops the repeat processing after processing a designated instruction in a N+1 th repeat processing, independently of an operation specified by an instruction being executed, said data processor comprising:

a detecting unit ~~means implemented by hardware,~~ for detecting ~~a break of repeat processing in said repeat block independently of an operation specified by an instruction being executed~~ that a processing instruction is said designated instruction and the repeat processing breaks after said designated instruction has been completed;

an instruction processing sequence switching unit to switch the instruction processing sequence to a first instruction within the repeat block after a last instruction in the repeat block has been completed when the repeat processing is made to continue by a detection result of said detecting unit; and

an instruction execution inhibit unit ~~means responsive to the detection of said break of said repeat processing by said detecting means~~ to inhibit execution of ~~remaining~~ following instructions after said specific instruction within [[in]] said repeat block,

wherein said detecting unit includes a detecting part that detects the processing is said N+1 th repetition of said repeat block and another detecting part

that detects the processing instruction is said specified instruction based on address information of the processing instruction and address information related to said specified instruction which is designated beforehand ~~means is means for deciding whether said repeat processing breaks, based on an address of an instruction that is executed during said repeat processing of said repeat block~~.

8. (Canceled)

9. (Canceled)

10. (Canceled)

11. (Currently Amended) A data processor with a hardware repeat function which executes ~~a program including~~ a repeat block composed of plural instructions ~~and processed repeatedly~~ N times (N is an integer equal to or more than 0) repeatedly, and stops the repeat processing after processing a designated instruction in a N+1 th repeat processing, independently of an operation specified by an instruction being executed, said data processor comprising:

a detecting unit ~~means implemented by hardware,~~ for detecting that a processing instruction is said designated instruction and the repeat processing breaks after said designated instruction has been completed;

an instruction processing sequence switching unit to switch the instruction processing sequence to a first instruction within the repeat block after a last instruction in the repeat block has been completed when the repeat processing is

made to continue by a detection result of said detecting unit ~~a break of repeat processing in said repeat block independently of an operation specified by an instruction being executed~~; and

an instruction execution inhibit unit ~~means responsive to the detection of said break of said repeat processing by said detecting means~~ to inhibit execution of ~~remaining~~ following instructions after said specified instruction within [[in]] said repeat block,

wherein said detecting unit detects ~~means is means for deciding~~ whether said repeat processing [[breaks,]] is completed or not based on a number of instructions ~~to be executed~~ which are processed during repeat processing of said repeat block, and includes a ~~wherein said detecting means has~~ first counter which counts ~~count means for counting~~ a number ~~of repetitions of~~ to perform the repeat processing of said repeat block and a second counter that counts ~~count means for counting the~~ a number of processed instructions in said N+1 th ~~executed during each~~ repeat processing ~~of said repeat block~~, and

wherein said detecting ~~means decides that~~ unit detects completion of said repeat processing ~~breaks~~ when a ~~count number~~ counter value of said first ~~count means~~ counter reaches a first predetermined value and [[the]] a ~~count number~~ counted value of said second ~~count means~~ counter reaches a second predetermined value ~~in a last~~ at the N+1 th repeat processing of said repeat block.